1E7903

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M. Tech. (Sem.I) (Back) Examination, April - 2009
Computer Science & Engineering
9CPC03 Architecture of High Performance Computer System

Time : **3** Hours] [Total Marks : **80**
[Min. Passing Marks : **27**

*Attempt any **five** questions. Marks of questions are indicated against each question. Draw neat and comprehensive sketches wherever **necessary** to clearly illustrate your answer. Assume missing data suitably if any and specify the same.*
*All questions carry **equal** marks.*

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. Nil 2. Nil

1 (a) What are the subsystems of a computer system? Carefully describe the aspects of each subsystems which need to be improved to increase the performance of computer system and discuss the trade offs, if any.

(b) What do you understand by following measures of performance CPI, MIPS, MFLOPS, DHRYSTONE and TPS. Carefully explain the merits and limitations of each measure.

2 (a) What is an instruction pipeline? Name the different stages of an instruction pipeline. How do the static and dynamic, synchronous and asynchronous, deep and shallow pipelines differ? Then explain the situations in which an instruction pipeline can stall?

(b) Consider the following reservation table for a pipeline :

(i) Find its forbidden latencies
(ii) Draw its state transition diagram
(iii) List its simple cycles and greedy cycles
(iv) Find its optimal constant latency cycle and minimum average latency.

	1	2	3	4
S_1	X			X
S_2		X		
S_3			X	

3 (a) A computer has a main memory of 1 GB and two caches of 8KB each, assume a block size of 2 KB.
(i) How many lines are there in each cache?

(ii) Assuming direct mapping, which memory blocks will map to the cache lines in the construction cache and which ones will map to the cache lines in the data cache?

(iii) Describe the mapping when the caches are 2 way set associative.

(iv) Discuss the merits and demerits of directly mapped, 2 way set associative and fully associative caches.

(b) Explain the locality of reference and its types. Describe the 90-10 rule and its relation to the locality of reference. Briefly describe the policies to update the cache memory from the main memory and the main memory from the virtual memory on a read or write miss. Point out the differences in these two cases, if any.

4 (a) What do you understand by the ILP and instruction processing hazards? Carefully explain different types of data hazards and control hazards. Then discuss the role of the branch target buffer and the branch prediction buffer in reducing the execution delay due to the control dependency.

(b) Carefully distinguish :

(i) Super pipelined and super scaler processors

(ii) Scaler and vector processors

(iii) UMA and NUMA architecture

(iv) SIMD an MIMD architecture.

5 (a) Describe the architecture of Pentium processor in relation with the various registers used by the programmes and by the processor in managing its operations and cache memory.

(b) Describe the pipeline used by pentium processor and discuss carefully how does it perform the integer and floating point operations. Also describe the super scaler operations of this CPU.

6 (a) What do you understand by hyperthreading? Carefully explain how this technology has been incorporated in the pentium processor.

(b) What is MMX technology? Carefully discuss the hardware and the new instructions which have been incorporated into Pentium Processor to implement this technology.

7 Write short notes on characteristic and performance of :

(i) RISC processors

(ii) CISC processors.