8E4093

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B. Tech. VIII Sem. (Main/Back) Exam., April, 2015
Electronics & Communication Engineering
8EC4.2 VHDL
Common for 8EX4.2 & 8EC4.2

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.

1. NIL 2. NIL

UNIT – I

Q.1 (a) Explain the history of various hardware description language. [6]

(b) Draw the schematic for ASIC design flow and explain every step in brief. [10]

OR

Q.1 (a) Differentiate between behavioral and structural style of modeling using suitable example. [10]

(b) Explain the following:- [6]

(i) Entity declaration

(ii) Architecture declaration

UNIT – II

Q.2 (a) Write VHDL code for 2 to 1 multiplexer using structural style modeling. [6]

(b) Write VHDL code for 2-input Ex-NOR gate design with minimum number(s) of 2-input NAND gate (only) as a component using structural modeling. [10]

OR

Q.2 Write hierarchical code for 16 to 1 multiplexer using structural modeling. [16]

UNIT – III

Q.3 (a) Draw FSM for (i) D-Flip Flop (ii) J-K Flip Flop & write VHDL code. [12]

(b) Write about concurrent, sequential and concurrent plus sequential VHDL statements. [4]

OR

Q.3 (a) Write VHDL code for modulo-10 up counter with synchronous reset. [10]

(b) Compare level triggered & edge trigger systems. [6]

UNIT – IV

Q.4 (a) Draw FSM and write VHDL code for a system which has a single bit input 'X' and two single bit outputs 'Y' and 'Z'. The output of system is asserted logic 1 to 'Y' and 'Z' when system detects input stream of serial bits 1001 or 1010 respectively. [16]

OR

Q.4 (b) Write VHDL code for serial adder. [8]

(b) Compare Mealy & Moore Type FSM. [8]

UNIT – V

Q.5 Explain the following:-

(a) Clock Synchronization [8]

(b) Design example of divider [8]

OR

Q.5 Q.5 Explain the following:-

(a) Memory organization [8]

(b) CPU organization [8]
