

**4E2149**

Roll No. : \_\_\_\_\_

Total Printed Pages : **4****4E2149****B. Tech. (Sem. IV) (Main / Back) Examination, June/July - 2013**  
**4EX2 Electrical Electronics***Digital*Time : **3 Hours**[Total Marks : **80**[Min. Passing Marks : **24***Attempt any five questions, selecting one question from each unit.**All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.**Units of quantities used/calculated must be stated clearly.*Use of following supporting material is permitted during examination.  
(Mentioned in form No. 205)1. NIL2. NIL**UNIT - I****1 (a)** Perform the following operations using 2's complement :

(i)  $(1ABC)_{16} + (1DEF)_{16}$

(ii)  $(+43)_{10} - (-53)_{10}$

(iii)  $(3E91)_{16} - (1F93)_{16}$

**2×3****(b)** Derive the Boolean expression for a 2 input EX-OR logic gate to realize with two input NAND gate without using complemented variables. Also, draw the circuit diagram.**4****(c)** A 12-bit Hamming code word containing 8-bits of data and 4 parity bits is read out from memory. What will be the original 8-bit word if the 12-bit read out is as follows :

(i) 1100 1010 0110

(ii) 0011 0110 0101

**3×2****OR****4E2149]****1****[Contd...**

- 1 (a) Explain how errors are detected using :  
 (i) Check sums  
 (ii) Block parity  
 4
- (b) What is reflective code ? With the help of an example, explain the differences between the reflective and sequential code.  
 4
- (c) A 16-bit data word given by 1001100001110110 is to be transmitted by using a fourfold repetition code. If the data word is broken into four blocks of four bit each, then write down the transmitted bit stream.  
 8

## UNIT - II

- 2 (a) Why ECL is called non-saturating device ? What is the main advantage accruing from this ? With help of relevant circuit diagram briefly describe the operation of ECL OR / NOR logic.  
 6
- (b) Show that in a totem pole TTL NAND gate, transistor  $Q_2$  and  $Q_3$  cannot conduct simultaneously.  
 6
- (c) Why it is not recommended to leave the unused logic inputs floating ? What should be done to such inputs in case of TTL and CMOS logic gate families.  
 4

## OR

- 2 (a) The data sheets of a Quad two-input AND gate specifies the propagation delay and power supply parameters as ;  
 $I_{CC} = 5.0mA$ ,  $I_{CCH} = 18mA$  (for all four gates);  $I_{CCL} = 32mA$  (for all four gates);  $t_{PLH} = 4.5ns$  and  $t_{PHL} = 5ns$ . Determine the speed power product specification.  
 10
- (b) What in a logic family, decides the fan-out, speed of operation, noise immunity and power dissipation.  
 6

## UNIT - III

- 3 (a) Write down the minterm and maxterm Boolean expression given by  $f(A, B, C) = \pi 0, 3, 7$ .  
 8



- (b) Reduce  $\pi M(1, 2, 3, 5, 6, 7, 8, 9, 12, 13)$  and implement it in universal logics.

8

OR

- 3 (a) Using the Quinn-McCluskey method of tabular reduction, minimize the given combinational signal output function.

$$f(A, B, C, D) = \sum M(0, 1, 5, 7, 8, 10, 14, 15)$$

8

- (b) Obtain the minimal POS expression for :

$$f = \pi M(0, 1, 4, 5, 9, 11, 13, 15, 16, 17, 25, 27, 28, 29, 31) \cdot$$

$$\cdot d(20, 21, 22, 30)$$

8

## UNIT - IV

- 4 (a) If the CARRY GENERATE  $G_i$  and CARRY PROPAGATE  $P_i$  are redefined as  $P_i = (A_i + B_i)$  and  $G_i = A_i B_i$ . Show that CARRY output  $C_{i+1}$  and SUM output  $S_i$  of full adder can be expressed as

$$C_{i+1} = (\overline{C_i} \overline{G_i} + \overline{P_i}) = G_i + P_i C_i \text{ and } S_i = (P_i \overline{G_i}) \oplus G_i.$$

8

- (b) Design the following :

- (i) 32 : 1 MUX using two 16 : 1 MUX's one 2 : 1 MUX.  
(ii)  $10 \times 1K$  decoder using 8 : 256 decoder and additional logics.

4×2

OR

- 4 (a) Implement the following multiple outputs combinational logic circuits using 3 to 8 line decoder circuitry :

$$F_1 = \sum m(0, 1, 2, 6)$$

$$F_2 = \sum m(2, 4, 6)$$

$$F_3 = \sum m(0, 1, 5, 6)$$

8

- (b) If the minuend, subtrahend and BORROW-W bits are respectively applied to Augend, Addend and CARRY-W inputs of a full adder, prove that the sum output of full adder will produce correct DIFFERENCE output.

8



## UNIT - V

- 5 (a) Determine the function performed by the circuit given in fig. 5 (a). Referring to circuit, write its count sequence if it is initialize at 0000. Also draw the timing sequence.

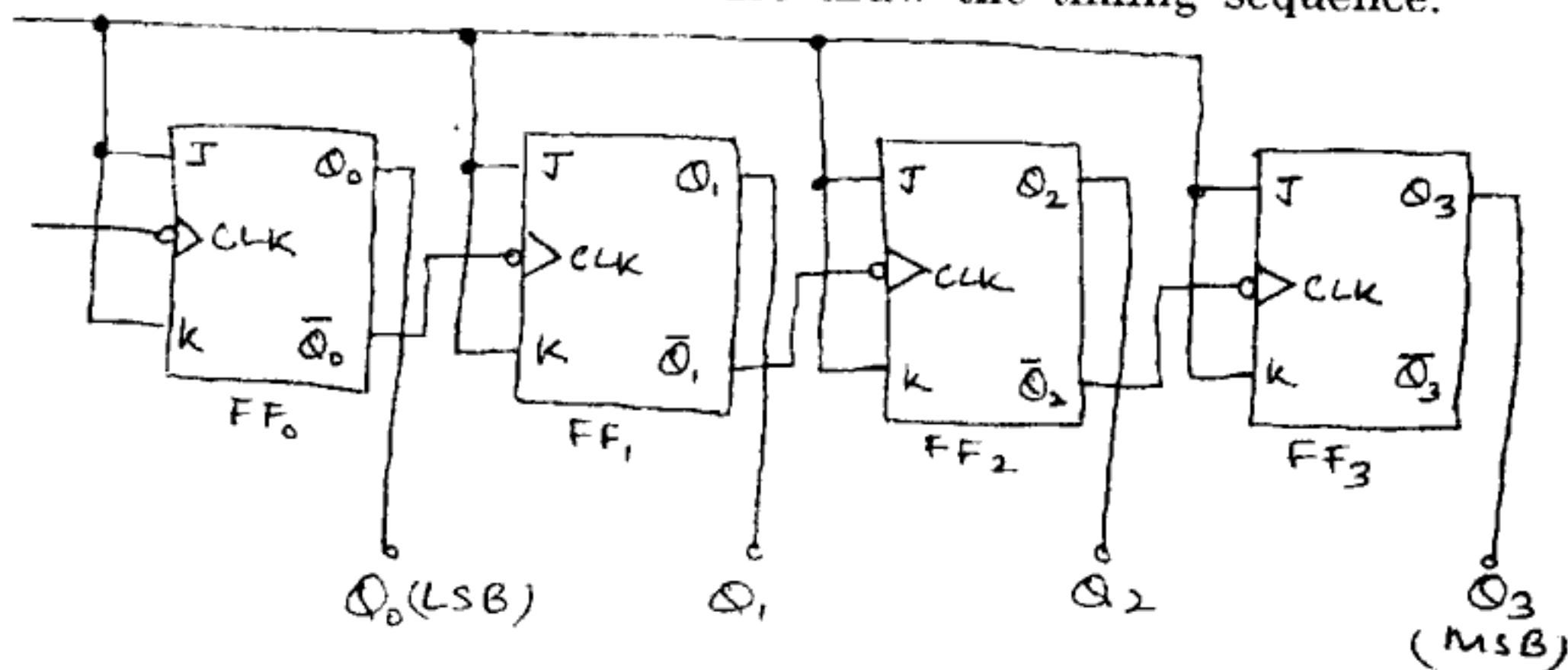


Figure 5 (a)

- (b) Why is the maximum usable clock frequency in case of a synchronous counter independent of the size of counter.

10

6

OR

- 5 The 100 KHz square waveform given in the figure 5 (b) is applied to clock input of flip flop given in figure 5 (c) and 5 (d). If the Q output is initialize at '0', draw the output waveform in two cases. Also determine the frequency of Q output in these two cases.

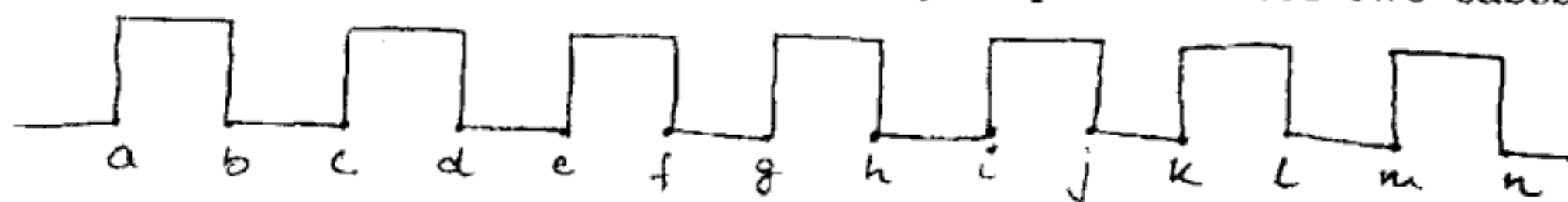


Figure 5 (b)

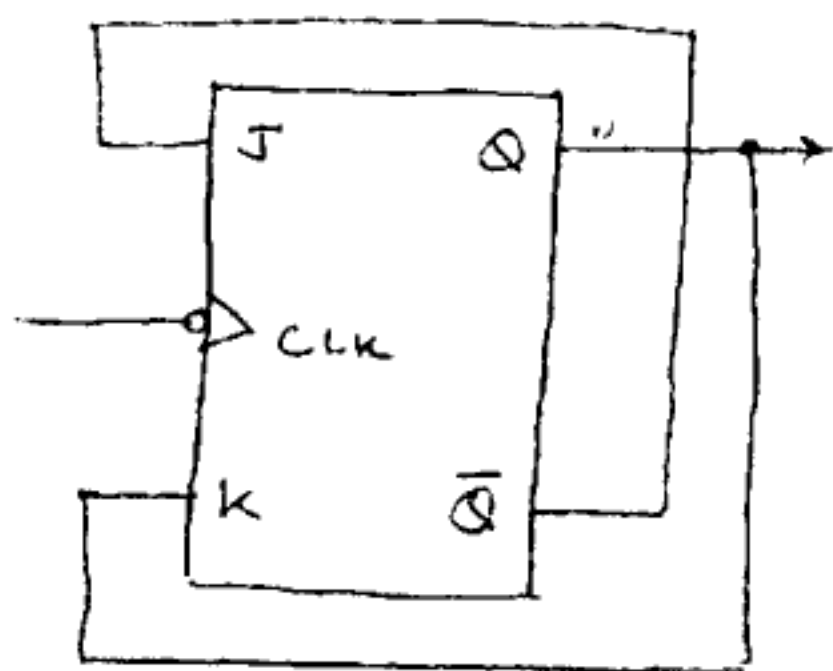


Figure 5 (c)

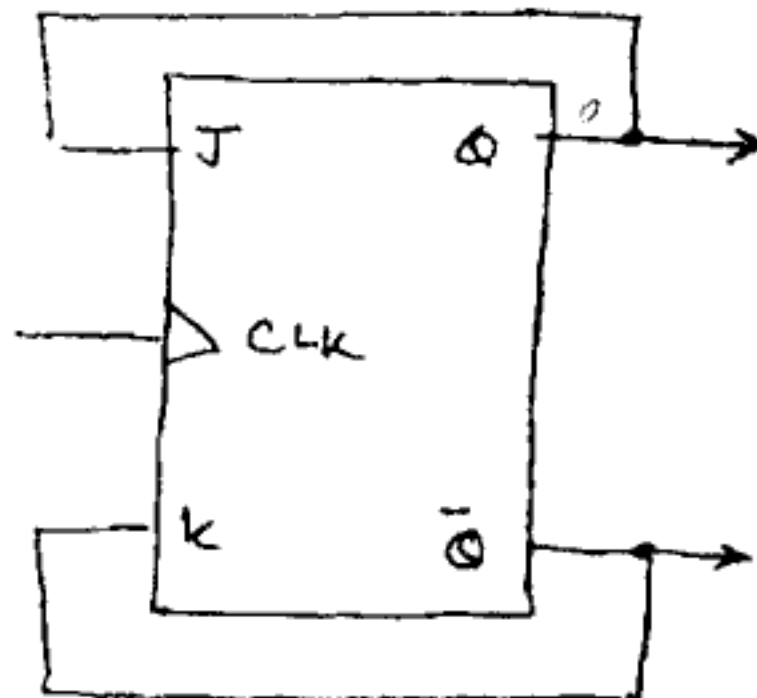


Figure 5 (d)

16

