4E2109

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B. Tech. IV-Sem. (Main/Back) Exam; April-May 2017

Electrical Engg.

4EE1(O) Power Electronics - II

Time : 3 Hours **Maximum Marks : 80**

Min. Passing Marks : 26

Instructions to Candidates :-

*Attempt any **five questions**, selecting **one question** from **each unit**. All Questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*
Units of quantities used / calculated must be stated clearly.
Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

1 (a) What are the advantages of negative feedback in amplifiers ? Derive the input impedance R_{if} of a voltage series and current shunt feedback amplifier.

(b) An amplifier has a voltage gain of 4000. It's input impedance is 2K and output impedance is 60 K. Calculate the voltage gain, input and output impedance of the circuit is 5% of the feedback is fed in the form of series negative voltage feedback.

OR

1 (a) Explain the concept of feedback with the help of block schematic of a signal loop feedback amplifier. Derive expression for the transfer gain with feedback.

(b) Draw the circuit diagram of a two stage amplifier employing current shunt feedback and obtain the expression of its gain with feedback.

UNIT - II

2 (a) What is the Barkhausen criterion for the feedback oscillators ? Explain the principle of working of Colpitts oscillator.

(b) What type of feedback is employed in oscillators ? Explain how amplitude and frequency stability are improved in an oscillators.

OR

2 (a) Why are the RC oscillators preferred for the generation of low frequencies ? Draw a neat circuit diagram of a phase shift oscillator using BJT. Derive an expression for its frequency of oscillation.

(b) In a Hartley oscillator, L_1 = 15 mH and C = pF. Calculate L_2 for a frequency of 168 kHz. The mutual inductance between L_1 and L_2 is 5 μH. Also find the required gain of the transistor to be used for the oscillator.

UNIT - III

3 (a) What is the mean by CMMR ? Derive the expression for CMMR in an emitter coupled differential amplifier.

(b) How a differentiator circuit can be designed using an ideal operation amplifier ? Explain.

OR

3 (a) Draw and explain logarithmic and antilog amplifier by using operation amplifier. Derive the expression of logarithmic amplifier.

(b) Explain the slew rate. For an operation amplifier having a slew rate of 3 v/μsec. What is the maximum closed loop voltage gain that can be used when the input signal varied by 0.4 v in 12 μsec ?

UNIT - IV

4 (a) Define the following term of D/A conversion :
(1) Resolution
(2) Accuracy
(3) Monotonicity
(4) Conversion time.

(b) Draw and explain the series emitter follower regulated power supply circuit.

OR

4 (a) Draw and explain the functional diagram of IC 555 timer and explain an application with the help of circuit diagram.

(b) Write short note on three terminal monolithic regulator.

UNIT - V

5 (a) Define the conversion efficiency. Compare maximum efficiency of a series fed and transformer coupled class A signal transistor power stage.

(b) Show that optimum conversion efficiency possible in class B push pull amplifier is 78.5% and also explain the main drawback of class B configuration in power amplifier.

OR

5 (a) Write short note on complementary symmetry power amplifiers.

(b) Prove that in class A amplifier if distortion is 10 percent power gain to the load is increased by 1 percent

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