3E1147

Roll No. Total No of Pages: 3

3E1147

B. Tech. III - Sem. (Main / Back) Exam., Dec. 2019
PCC Electronics & Communication Engineering
3EC4-04 Digital System Design
Common For EC, EI

Time: 3 Hours **Maximum Marks: 120**

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and four questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 Find value of x for following equation:

$(135)_x + (531)_x = (666)_x$

Q.2 Convert $(1011)_{\text{gray code}}$ to excess-3 code.

Q.3 Find the sum of $(1.98)_{10} + (4.86)_{16}$.

Q.4 State the difference between flip flop and latch.

Q.5 Write the excitation table of RS flip flop.

Q.6 Define figure of merit for logic family.

Q.7 How many Boolean functions can be made from 3 variables?

Q.8 Write a VHDL code for $y=\overline{A}\overline{B}$ in structural style of modelling.

Q.9 How many flip flops are required to design modules 20 counter?

Q.10 If the present output of 4 – bit twisted ring counter is 1011, then find its output after 6 clock cycles.

PART – B

(Analytical/Problem solving questions) **[5×8=40]**

Attempt any five questions

Q.1 How Ex-OR gate is used in parity bit generation and error detection at transmitter and receiver respectively? Explain using an example of 8-bit data.

Q.2 Convert following canonical form into standard form using tabulation method

$$Y=\sum m\,(4,5,6,11,13)+d\sum(0,2)$$

Q.3 Explain the procedure for conversion of RS flip flop into JK flip flop.

Q.4 Write the help of neat circuit diagram explain the interfacing of various logic families.

Q.5 Implement the following Boolean functions:

(i) $Y=\overline{AB+CD}$ using CMOS

(ii) $Y = AB+C$ using PMOS

Q.6 Write a VHDL code for full adder in structural style of modelling.

Q.7 What is FSM? State the difference between Mealy and Moore state machines.

[1540]

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[4×15=60]**

Attempt any four questions

Q.1 (a) What are prime, essential and redundant implicants? Explain with an example.

(b) Signals A, B, C, D and $\overline{A}$ are available. Using only 8:1 mux and no other gate, implement the expression $F(A, B, C, D) = BC + AB\overline{D} + \overline{A}\,\overline{C}D$

Q.2 The state diagram of a FSM is given below (Fig 1).

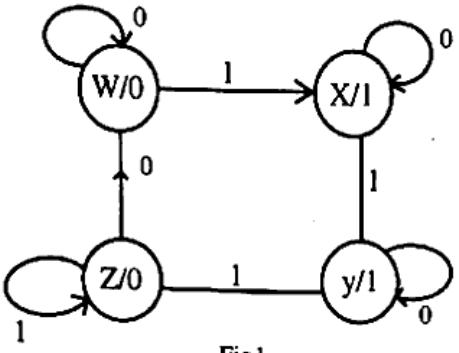

Fig 1

Show its state table, state assignment table and final implemented logic.

Q.3 Design a synchronous counter using JK flip flop to generate following sequence

0,7,5,3,2,1

Also write its state table, state assignment table and final implemented logic.

Q.4 (a) Design the 4-input priority encoder with truth table and draw its logic diagram.

(b) Draw and explain the logic diagram of BCD adder using two 4 bit adders and a correction detection circuit.

Q.5 Write a short note on following :

(i) FPGA

(ii) PLA

(iii) CPLD

(iv) PAL
