8E4093

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B. Tech. VIII Semester (Main/Back) Examination-2014

ELECTRONICS & COMMUNICATION # 8EC42

# VHDL

Time : 3 Hours | Min. Passing Marks : 24 | Total Marks : 80

*Instruction to Candidates :*

*Attempt any five questions, selecting one question from each unit. All questions carry equal marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.)*

## Unit-I

1. (a) What is VHDL? Explain its capabilities and features. [8]
   (b) Explain various type of hardware description languages. [8]

OR

1. (a) Define synthesis and simulation in VHDL. Differentiate between them using one example. [6]
   (b) Explain VHDL statement using one example for each.
   (i) Concurrent assignment statement
   (ii) Delay define in VHDL
   (iii) Case statement.
   (iv) Loop statement.
   (v) IF statement. [2×5=10]

## Unit-II

2. (a) Write VHDL code for 16:1multiplexer using 4×1 multiplexer. Draw the circuit in block diagram form. [8]
   (b) Implement a 4 to 16 binary decoder using 2 to 4 decoder, write its VHDL code using generate statement. [8]

OR

2. (a) Using a conditional signal assignment statement, write VHDL code for 8-to-3 encoder. [8]
   (b) Write a VHDL code for a BCD to 7-segment code converter. [8]

## Unit-III

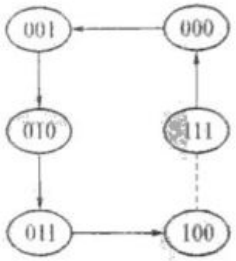
3. (a) Write a VHDL code for two-digit BCD counter. [6]
   (b) Design a three bit binary counter that counts upward, show its state diagram and write VHDL code for it. [10]

OR

3. (a) Write VHDL code for positive edge triggered D flip-flop., [8]
   (b) Write VHDL code for 8 bit-shift register. [8]

## Unit-IV

4. (a) Write VHDL code for the serial adder circuit. [6]
   (b) Identify the machine weather Mealy or Moore type whose state diagram is:




Design its VHDL code as well as a DEF implementation circuit. [10]

OR

4. (a) Draw the state diagram for an FSM with input x and output y such that y is high for previous four input values are 1001 or 1111, let input is:
   X:010111110011 001111
   Write its VHDL code. [10]
   (b) Enumerate the difference between Mealy and Moore type Fsms. [6]

## Unit-V

5. What is memory organization? Give diagram of single SRAM cell and write the code in VHDL. [16]

OR

5. Write short notes on :
   (a) Clock synchronization
   (b) Multiplier. [2×8=16]