

<b>7E7084</b>	Roll No.	Total No of Pages: <b>3</b>
<b>7E7084</b> <b>B. Tech. VII - Sem. (Back) Exam., Feb.-March - 2021</b> <b>Electronics &amp; Communication Engineering</b> <b>7EC5A VLSI Design</b>		

**Time: 2 Hours**

**Maximum Marks: 48**  
**Min. Passing Marks: 15**

*Instructions to Candidates:*

*Attempt three questions, selecting one question each from any three unit. All Questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.*

*Use of following supporting material is permitted during examination.*

*(Mentioned in form No.205)*

1. NIL

2. NIL

### UNIT- I

- Q.1 (a) Draw and write the working of enhancement mode PMOS with the help of input-output and transfer characteristics. [8]
- (b) Write the names and compare the three technologies used for the fabrication of CMOS transistor. [8]

**OR**

- Q.1 (a) What are the different factors affecting the threshold voltage of MOSFET? Derive the formula used. Also, derive the body effect coefficient. [8]
- (b) Draw MOS transistor circuit, model and explain the origination of each parameter. [8]

## UNIT- II

- Q.2 (a) Draw voltage transfer characteristics (VTC) of CMOS inverter and derive the expression for  $B_n/B_p$  ratio. [3]
- (b) Write the names of three types of power dissipation in CMOS logic circuits and derive the expression for total power dissipation. [3]

OR

- Q.2 (a) Design the following logic circuits using CMOS logic gate - [4]
- (i) 3 - input NAND gate
- (ii) S-R Flip-flop
- (b) Implement the Boolean expression  $F = a \cdot (b + b'c')$  using CMOS logic and also determine the size of each transistor using equivalent inverter transistor sizes. [4]

## UNIT- III

- Q.3 (a) Implement  $2 \times 1$  multiplexer using transmission gate and draw its layout. [8]
- (b) Draw Euler path and layout diagram for 3-input NOR gate and mark all the size/spacing using  $\lambda$  -rules. [8]

OR

- Q.3 (a) What is latch-up problem in CMOS? Draw and explain its physical origin, model and V-I characteristics. [8]
- (b) Write the names and explain the techniques used to prevent latch-up problem. [8]

## UNIT- IV

- Q.4 (a) Compare NORA and NP(ZIPPER) CMOS logic structures. [8]
- (b) Explain various circuit techniques used in domino CMOS circuits for solving charge sharing problem. [8]

**OR**

- Q.4 (a) Draw a circuit diagram of a DRAM cell and explain the following operations— [8]
- (i) Synchronous read mode
  - (ii) Asynchronous read mode
  - (iii) Leakage currents and refresh operation
- (b) Draw SRAM cell and explain its write and read operation with appropriate timing diagram. [8]

**UNIT- V**

- Q.5 (a) Draw VHDL/PLD based ASIC design flow block diagram. Explain each step involved. [8]
- (b) Write VHDL code for positive edge triggered S-R flip-flop. [8]

**OR**

- Q.5 (a) Write VHDL code for half adder in structural style. [8]
- (b) Write VHDL model for left to right shift register using enable input. [8]

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