3E1653

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B. Tech. III - Sem. (Main / Back) Exam., Dec. - 2018
Electronic Instrumentation & Control Engineering
3EI3A Digital Electronics
EE, EX, EC, EI, CS, IT, AI

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Find the unknown number – [4×2=8]

(i) $(123)_{10} + (?)_{10} = (BA)_{16}$

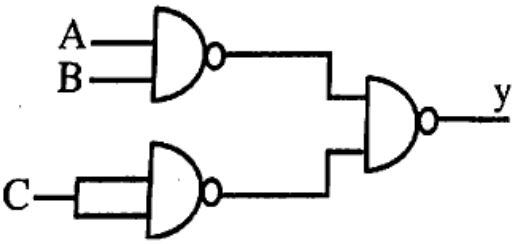
(ii) $(11000)_2 + (143)_8 = (?)_{10}$

(iii) $(1A)_{16} + (342)_8 = (\ )_4$

(iv) $(?)_2 + (102)_8 = (420)_{16}$

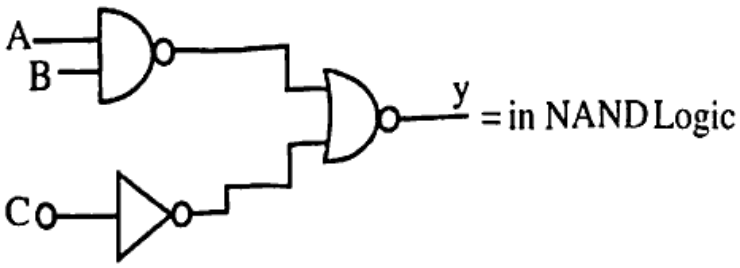
(b) Convert following – [2+2+4=8]

(i)

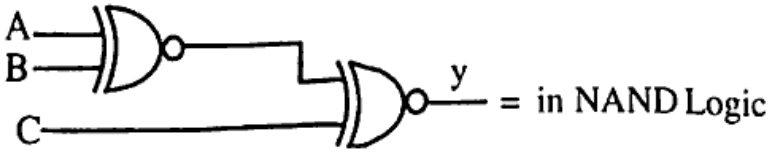


= in NOR Logic

(ii)



(iii)



OR

Q.1 (a) Convert following – [4×2=8]

(i) (1010) gray code → into excess – 3 code

(ii) $(1.204)_{10} = (\ )_2$

(iii) $(0.001)_2 + (1000)_8 = (\ )_{16}$

(iv) $(242)_8 + (2.42)_8 = (\ )_2$

(b) Define following – [4×2=8]

(i) Sign representation in Binary no.

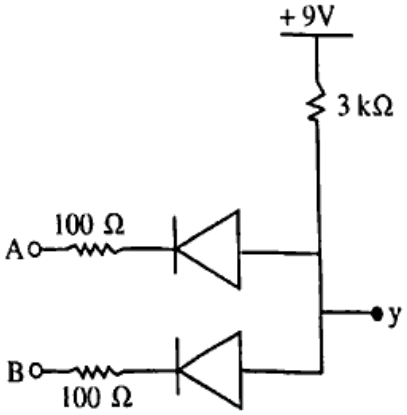
(ii) Negative logic

(iii) Universal logic

(iv) Fixed point representation

UNIT- II

Q.2 (a) Calculate the logic level for high and low output in logic circuit (fig – 2 (i)) [8]



Assume the diode drop is 0.7 volt and the standard input logic level are

0 → 0 volt

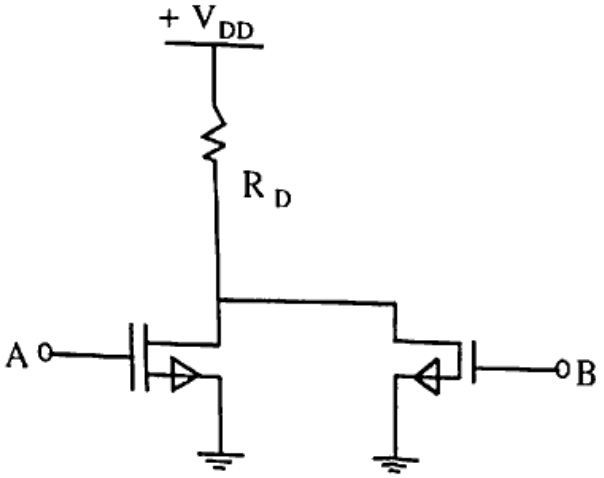
1 → 9 volt

Also explain the logic perfumed by this circuit.

(b) Explain the logic perfumed by the MOSFET circuit Fig – 2 (ii). Also discuss about the high and low voltage levels in this logic under following conditions- [8]

(i) $R_D = 100\ \Omega$ (Very Small)

(ii) $R_D = 100\ M\Omega$ (Very High)



OR

Q.2 (a) What is HTL? Design a 2 – input AND HTL gate to achieve noise margin of 2.5 volt. [8]

(b) Draw the circuit diagram of I^2L logic and explain its working. Where these logics are preferable? [8]

UNIT- III

Q.3 (a) Draw K – map for following and find the minimized logic expression for output. [4+4=8]

(i) $y = \Sigma m\ (2, 5, 6, 8, 12, 13, 14) + d\ (3, 9)$

(ii) $y = \pi\ m\ (0, 1, 2, 7) + d\ (4, 5)$

(b) Minimize following – [4+4=8]

(i) $y = \overline{(A + B)(\bar{C} + D)} + \overline{A\bar{B}C}$ using simplification.

(ii) $y = \Sigma\ (0, 1, 2, 6, 7)$ using Quine – McCluskey method.

OR

Q.3 (a) In a 4 – variable K – map there are following groups formed. [8]

(i) 2 – Quad (four entries)

(ii) 2 – two entries group.

Write all possible minimized logic expressions for it.

(b) Express following in – [2×2=4]

(i) $y = AB(\bar{C} + D)$ in POS

(ii) $y = (A + B) + \bar{C}D$ in SOP

(c) Discuss the role of don't care conditions in minimization. [4]

UNIT- IV

Q.4 (a) Draw the Block diagram of a serial 4 bit adder and calculates its total time taken in addition in terms of clocks. [8]

(b) Implement a 16 × 1 mux in terms of 2 × 1 mux. Also estimate its total delay from input to output. Compare this delay with a direct implementation of 16 × 1 Mux. [8]

OR

Q.4 (a) Design an octal to binary converter. [8]

(b) Draw the circuit diagram of a 2 bit multiplier. [8]

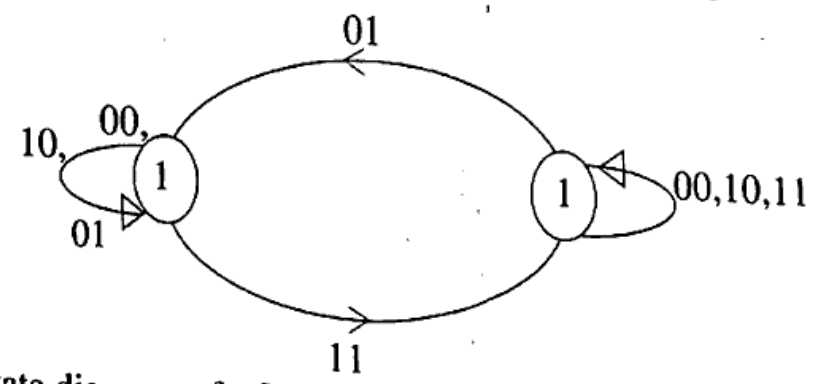
UNIT- V

Q.5 (a) Draw Synchronous Modulo – 7 Counter and explain its working. [8]

(b) Design a counter that count from 0 – 12 but skip 6, 7 and 9. [8]

OR

Q.5 (a) Draw the logic circuit for the state diagram given in fig – 5 [8]



(b) Draw state diagram of a JK and D – FF. Also discuss their inter conversion. [8]