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4 (a) What are heterogeneous processors? Explain internal structure of cognigine network processor (RCU).

3+7

(b) What is ~~IXP~~? Explain memory hierarchy for IXP 1200.

3+7

5 (a) Write a set of assembly language macros that use the scratchpad memory test and set operations to implement counting semaphores.

10

(b) Explain processor coordination via memory locking.

10

6 (a) Explain the internal architecture of Intel IXP 2400.

12

(b) What are the enhanced capabilities and facilities provided by the IXP 2400 ?

8

7 Write the short notes on any two of the followings :

(a) TCP splicing Algorithm

(b) RISC Vs CISC **rtuonline.com**

(c) Intel Dispatch Loop Macros.

