3E1653

Roll No. : _____ Total Printed Pages : 7

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B. Tech. (Sem. III) (Main/Back) Examination, December - 2017
Electronics & Communication Engg.
3EC3A Digital Electronics

Time : 3 Hours **Maximum Marks : 80**
Min. Passing Marks : 26

Attempt any five questions, selecting one question from each unit. All Questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used / calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. Nil 2. Nil

UNIT - I

1 (a) Find the 11's complement of following numbers :

(i) $(935)_{12}$ (ii) $(267)_{12}$ 6

(b) X and Y are successive digits in positional number system and $(XY)_r = (25)_{10}$ and $(YX)_r = (31)_{10}$. Determine the value of X, Y and r. 6

(c) A register contains 2's complement 10010110. What will be the contain of register if it is divided by 2. 4

OR

1 (a) Consider the signed binary number are $A = 01000110$ and $B = 11010011$ where B is in 2's complement form. Find the value of following Mathematical expression :

(i) $A + B$

(ii) $A - B$

(iii) $B - A$

(iv) $-A - B$ 8

(b) Why the gray code is also known as reflected code ? Write a brief note on gray code and its applications. 8

UNIT - II

2 (a) What do you understand by following properties of logic family :

(i) Fan out

(ii) Figure of merit

(iii) Noise margin

(iv) Current mode logic. 8

(b) Find the output boolean function (Y) in terms of A and B as shown in **Fig. 1**.

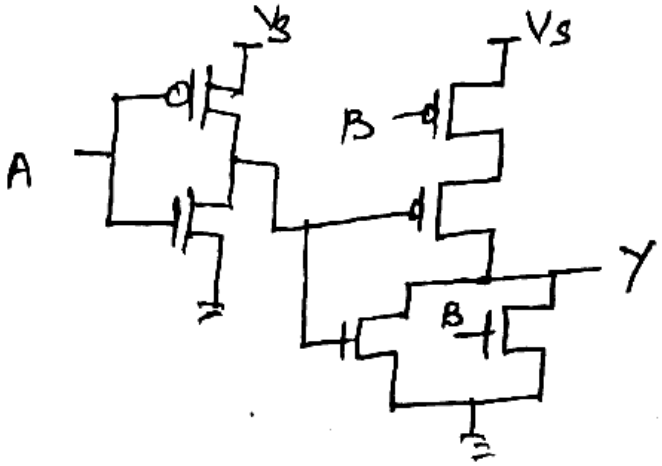

Fig. 1

8

OR

2 (a) A boolean function is implemented using NMOS logic family and shown in **Fig. 2**. How the output Y can be made 0 if C and D both values are 0. Also find implemented boolean function.

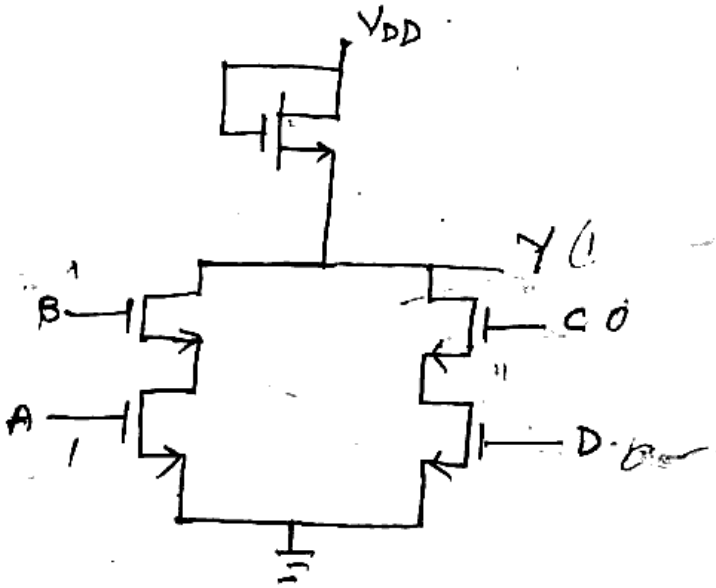

Fig. 2

8

(b) State the advantage of using totem pole output type TTL, over open collector output TTL. Also explain the tristate output logic type TTL. 8

UNIT - III

3 (a) Simplify the following boolean function using tabulation method :

$$F = \sum m\,(0, 1, 2, 8, 10, 11, 14, 15) \cdot d(9, 12).$$

10

(b) Simplify the following boolean function using K-map :

$$Y = (A + B)(A + \overline{C})(\overline{A} + \overline{B})(\overline{A} + C).$$

6

OR

3 (a) The logic gate G_1 and G_2 as shown in **Fig. 3** have propagation delay of 10 ns and 20 ns respectively. If input v_i makes an abrupt change from logic-0 to logic-1 at time $t = t_0$, then draw output waveform (V_0).

ns → nano second.

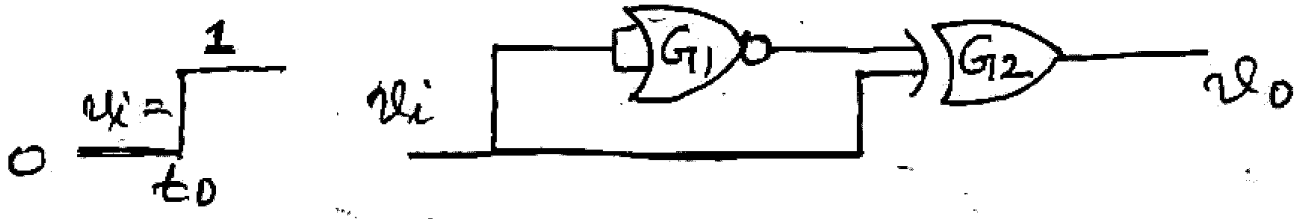

Fig. 3

8

(b) Minimize the following boolean function using K-map :

$$f(a, b, c, d) = \sum m\,(0, 1, 2, 8, 9) \cdot d(4, 10, 12)$$

8

UNIT - IV

4 (a) How many 3 : 8 line decoder with enable input are required to construct 6 : 64 line decoder without using any other logic ? Draw its block diagram also. 8

(b) Find the boolean function implemented by 4 : 1 mux as shown in **Fig. 4.**

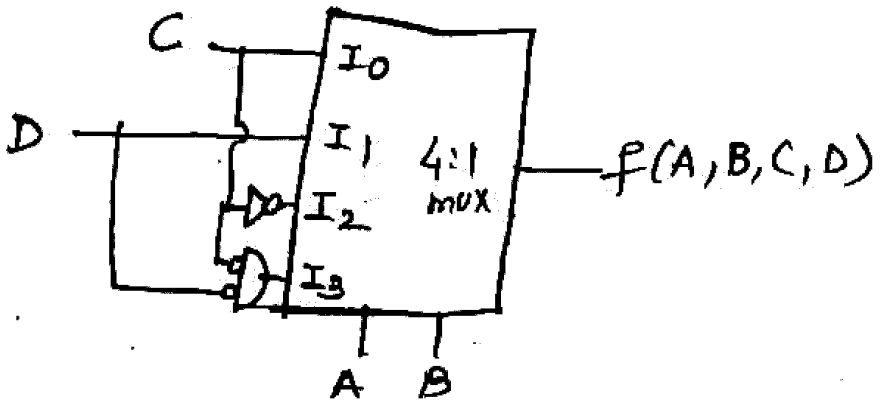

Fig. 4 8

OR

4 (a) Implement a full subtractor using two 4 : 1 multiplexer. 8

(b) Find the output of following decoder circuit as shown in **Fig. 5.**

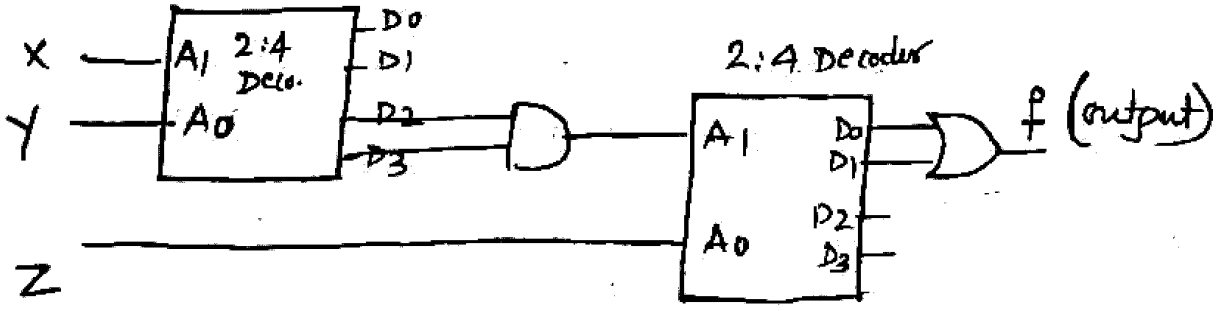

Fig. 5 4

(c) Find the output of 4 : 1 multiplexer as shown in **Fig. 6.**

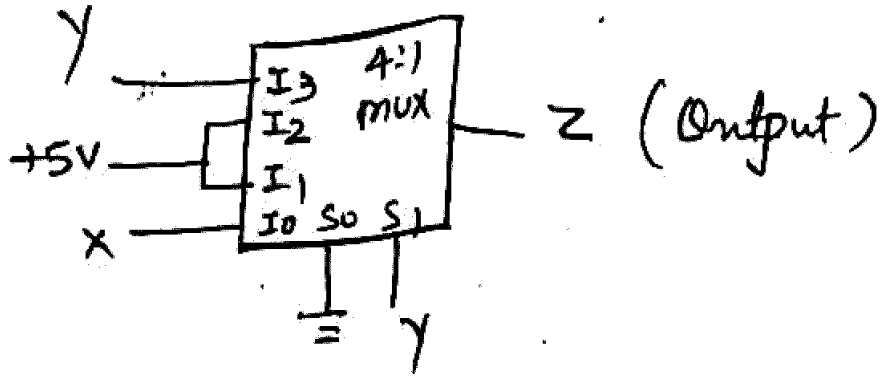

Fig. 6

4

UNIT - V

5 (a) State the difference between latch and flip flop.

4

(b) Explain the truth table, circuit diagram and working of universal flip flop.

4

(c) What are the counting states (Q_1, Q_0) for the circuit using D - flip flop as shown in **Fig. 7** ?

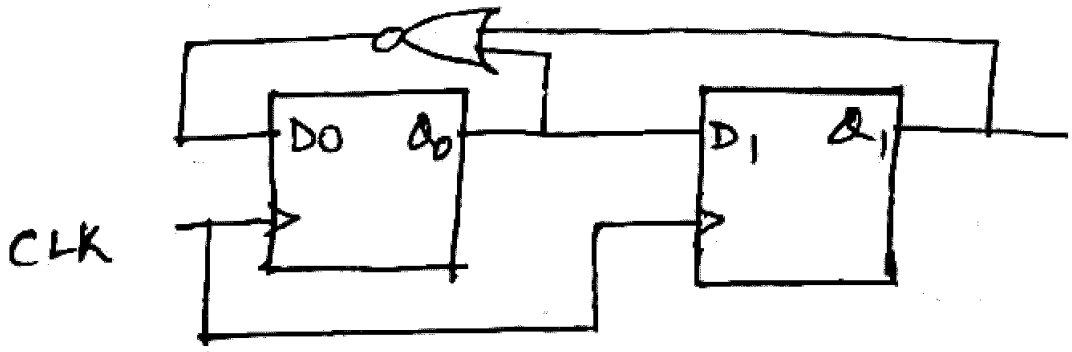

Fig. 7

Assume initial state (Q_1, Q_0) is 00.

8

OR

5 (a) Explain the procedure for conversion of JK flip flop to RS flip flop. 6

(b) What is race around condition ? How it can be avoided ? 5

(c) Design a binary counter with following binary sequence using D - flip flop : 0, 1, 3, 2, 6, 4, 5, 7 and repeat. 5